Product Specification

Product Name: VGM128064A3W01

Product Code: M00130

Customer
Approved by Customer
Approved Date:

Designed By	Checked By	Approved By	
		R&D	QA

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
E01	Initial release.	2009.04.14	
E02	Modify FPC.	2009.04.21	
E03	Correct the mistake of FPC drawing.	2009.04.23	
Y01	Updata content.	2009.06.04	

1 Overview

VGM128064A3W01 is an OLED monochrome128×64 dot matrix display module. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

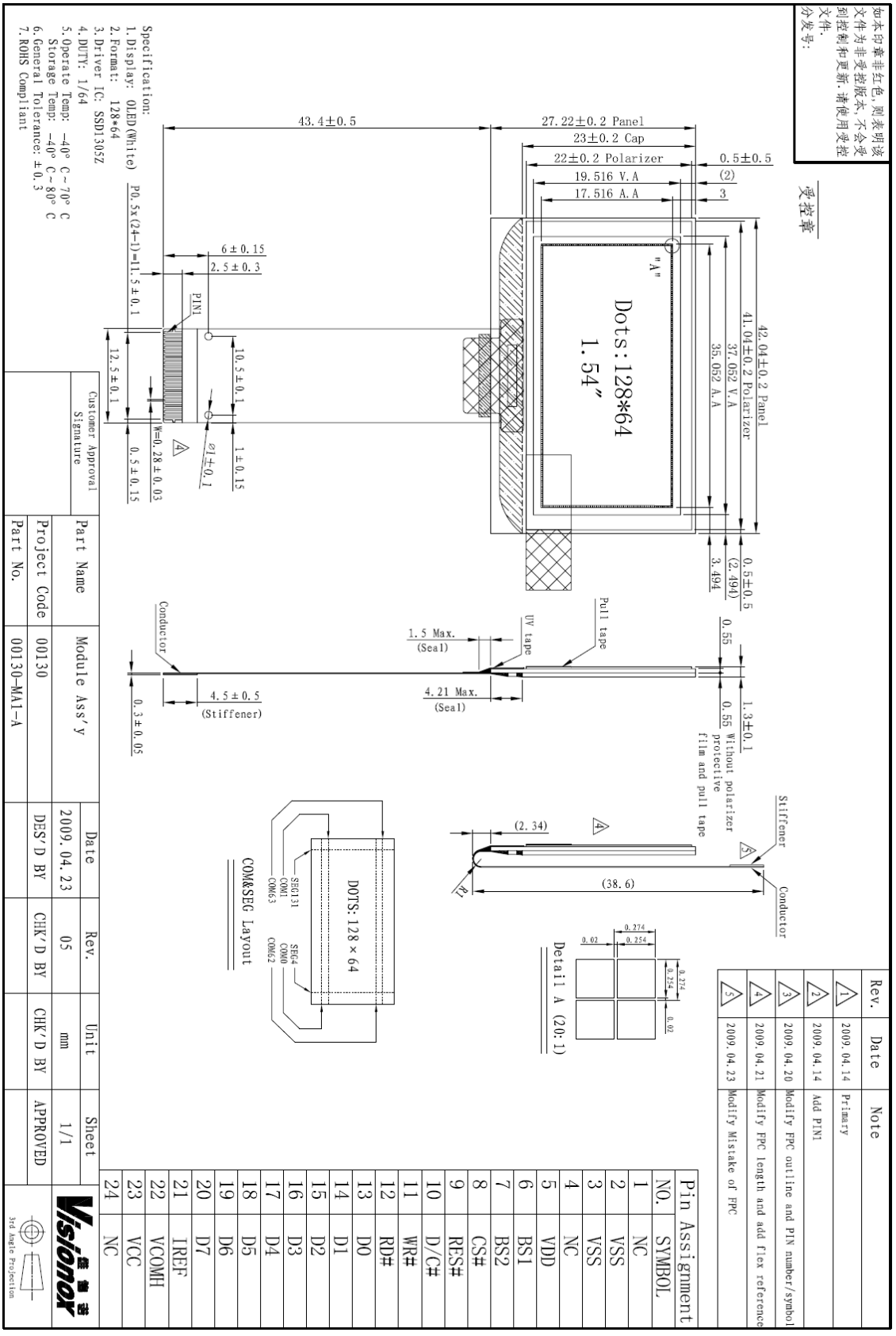
2 Features

- Display Color: White
- Dot Matrix: 128×64
- Driver IC: SSD1305Z
- Interface:8-bit 8080,8-bit 6800, SPI, I^2C
- Wide range of operating temperature: -40℃~70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×64(H)	-
2	Dot Size	0.254(W)×0.254 (H)	mm^2
3	Dot Pitch	0.274(W)×0.274 (H)	mm^2
4	Aperture Rate	86	%
5	Active Area	35.052(W)×17.516 (H)	mm^2
6	Panel Size	42.04(W)×27.22 (H)	mm^2
7	Module Size	According to the annexed mechanical drawing	mm^3
8	Diagonal A/A Size	1.54	inch
9	Module Weight	3.04±10%	gram

4 Mechanical Drawing



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分发号：

受控章

Rev.	Date	Note
1	2009.04.14	Primary
2	2009.04.14	Add PIN1
3	2009.04.20	Modify FPC outline and PIN number/symbol
4	2009.04.21	Modify FPC length and add flex reference
5	2009.04.23	Modify Mistake of FPC

Pin Assignment

NO.	SYMBOL
1	NC
2	VSS
3	VSS
4	NC
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	WR#
12	RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	NC

Part Name	Module Ass'y	Date	Rev.	Unit	Sheet
Project Code	00130	2009.04.23	05	mm	1/1
Part No.	00130-MA1-A	DES'D BY	CHK'D BY	CHK'D BY	APPROVED

Customer Approval Signature

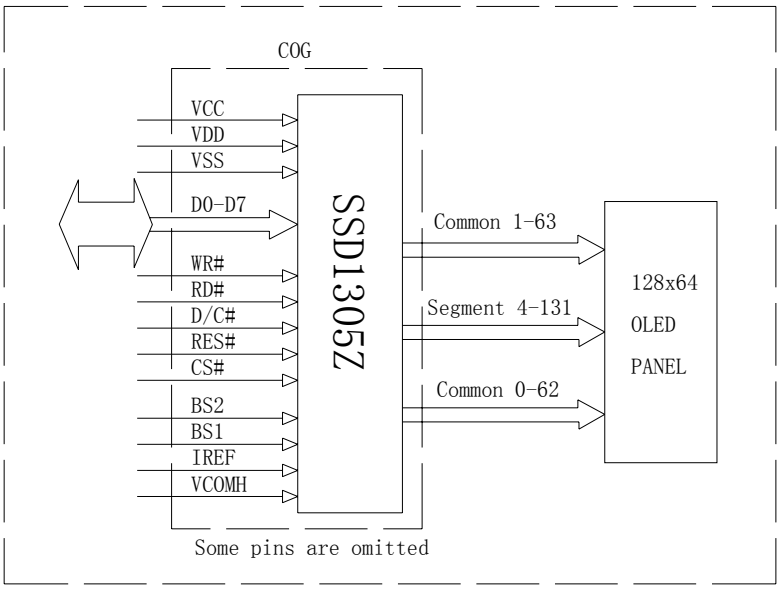
3rd Angle Projection

5 Module Interface

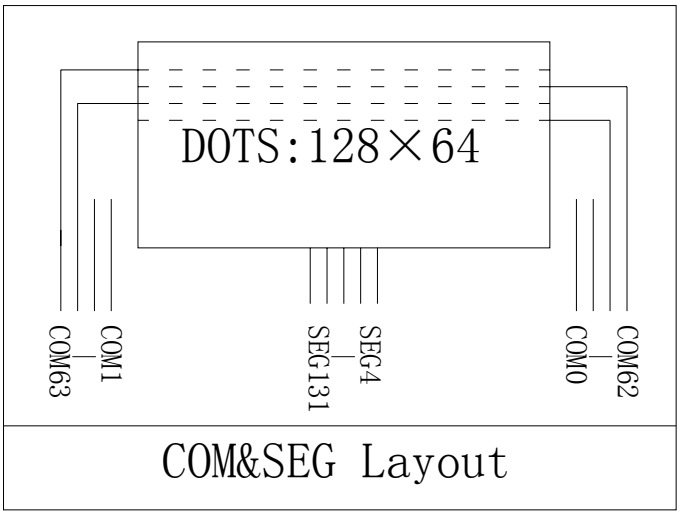
<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>2~3</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>4</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>5</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">MCU bus interface selection pins.
<table>
<tr><th>Pin Name</th><th>I²C Interface</th><th>6800-parallel interface (8 bit)</th><th>8080-parallel interface (8 bit)</th><th>Serial interface</th></tr>
<tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>Chip Select, active low. In I²C mode, this pin should be connected to VSS.</td></tr>
<tr><td>9</td><td>RES#</td><td>Reset, active low.</td></tr>
<tr><td>10</td><td>D/C#</td><td>H:Data; L :Command.In I²C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>11</td><td>WR#</td><td>8080: Write; 6800: Read/Write select pin; SPI or I²C:connected to VSS.</td></tr>
<tr><td>12</td><td>RD#</td><td>8080: Read; 6800: Read/Write enable pin; SPI or I²C:connected to VSS.</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>Data bus.
<table>
<tr><th>Pin Name / Bus Interface</th><th colspan="8">Data/Command Interface</th></tr>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit 8080</td><td colspan="8">D[7:0]</td></tr>
<tr><td>8-bit 6800</td><td colspan="8">D[7:0]</td></tr>
<tr><td>SPI</td><td colspan="5">Tie LOW</td><td>NC</td><td>SDIN</td><td>SCLK</td></tr>
<tr><td>I²C</td><td colspan="5">Tie LOW</td><td>SDA_{OUT}</td><td>SDA_{IN}</td><td>SCL</td></tr>
</table></td></tr>
<tr><td>21</td><td>IREF</td><td>This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>22</td><td>VCOMH</td><td>The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>23</td><td>VCC</td><td>Power supply for panel driving voltage.</td></tr>
<tr><td>24</td><td>NC</td><td>No Connection.</td></tr>
</table>

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	V_{DD}	-0.3	4.0	V	IC maximum rating
OLED Operating voltage	V_{CC}	0	16	V	IC maximum rating
Operating Temp.	Top	-40	70	℃	-
Storage Temp	Tstg	-40	80	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Logic Supply Voltage	V_{DD}	22±3°C, 55±15%R.H	2.4	3.0	3.5	V
OLED Driver Supply Voltage	V_{CC}	22±3°C, 55±15%R.H	12.5	13	13.5	V
High-level Input Voltage	V_{IH}	-	$0.8\times V_{DDIO}$	-	-	V
Low-level Input Voltage	V_{IL}	-	-	-	$0.2\times V_{DDIO}$	V
High-level Output Voltage	V_{OH}	-	$0.9\times V_{DDIO}$	-	-	V
Low-level Output Voltage	V_{OL}	-	-	-	$0.1\times V_{DDIO}$	V

Note : The V_{CC} input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1)	TBD	100	-	cd/m^2
Standby Mode Brightness		Standby Mode 10% pixels ON(2)	-	TBD	-	cd/m^2
Normal Mode Power Consumption	Pt	All pixels ON(1)	-	TBD	TBD	mW
Standby Mode Power Consumption		Standby Mode 10% pixels ON(2)	-	TBD	-	mW
C.I.E(White)	(x)	x,y(CIE1931)	TBD	TBD	TBD	-
	(y)		TBD	TBD	TBD	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : 13V
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/64

Note(2): Standby Mode test conditions are as follows:

- Driving voltage : 13V
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/64

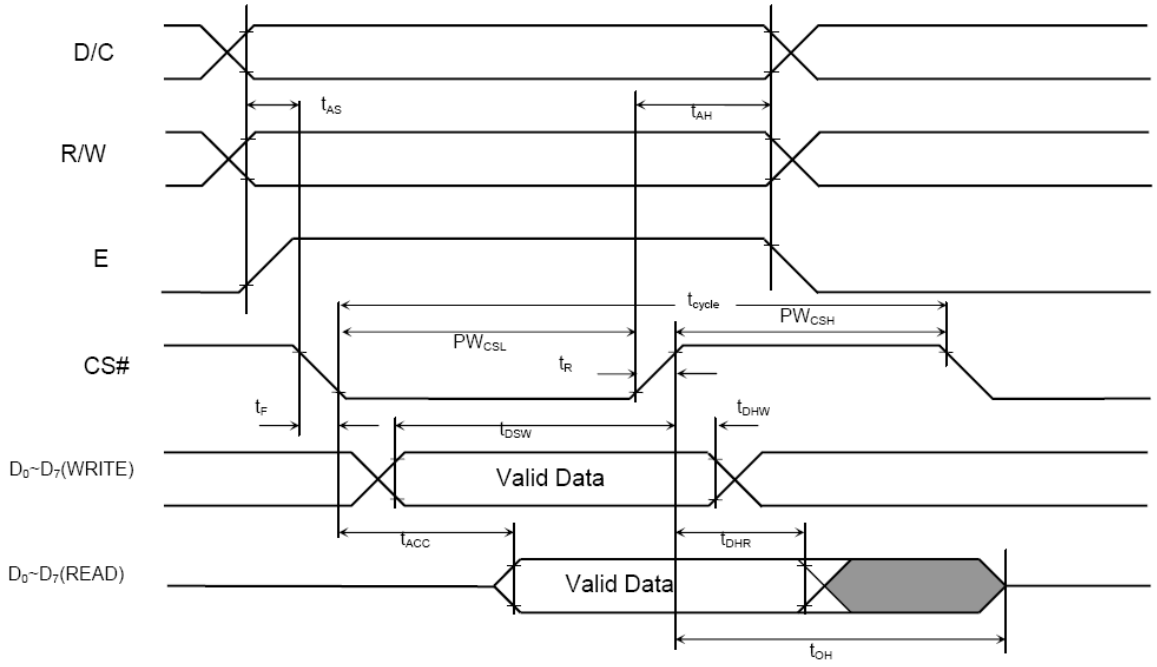
8.3 AC Electrical Characteristics

(1)6800-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics



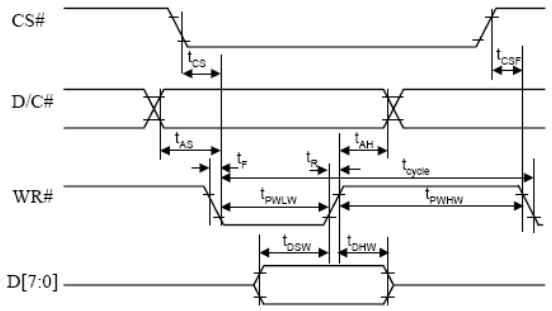
(2)8080-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

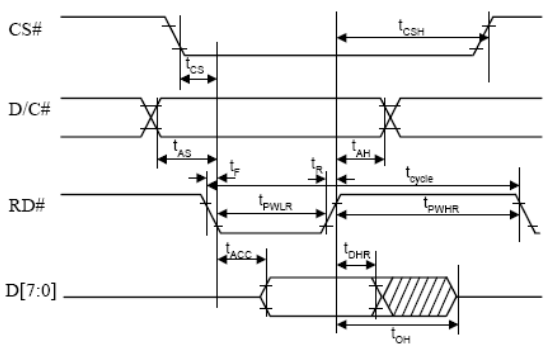
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)

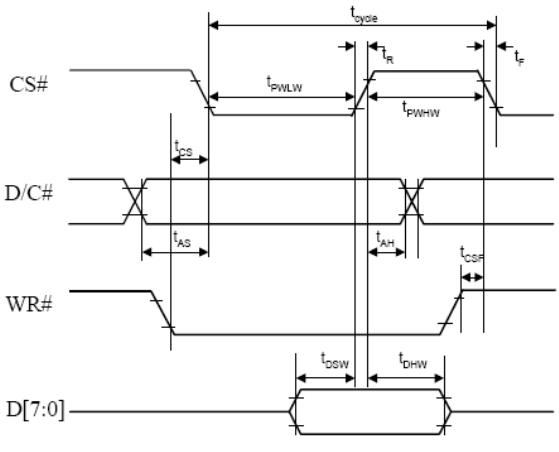


Read cycle (Form 1)

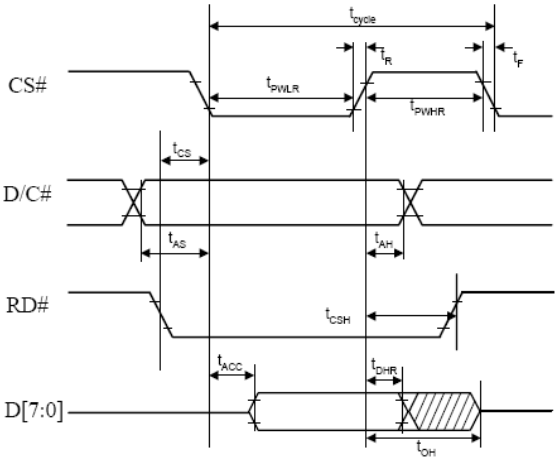


8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)

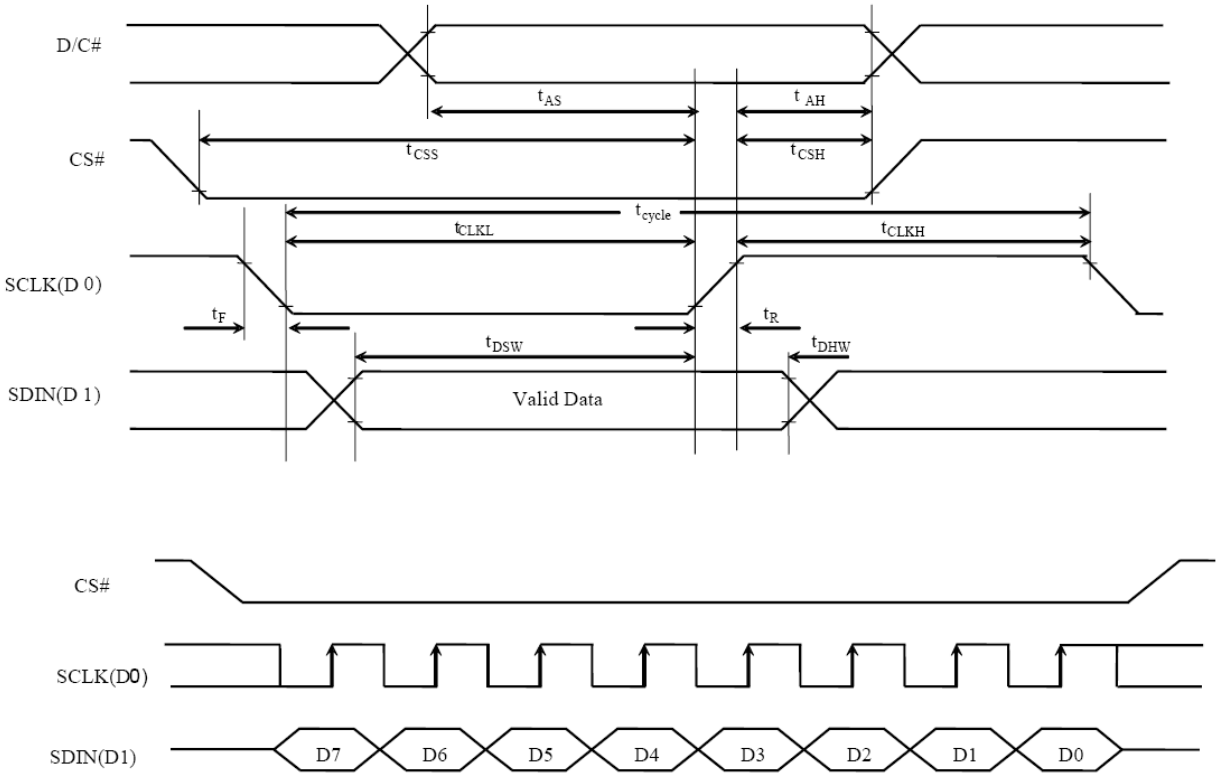


(3)Serial Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Serial interface characteristics

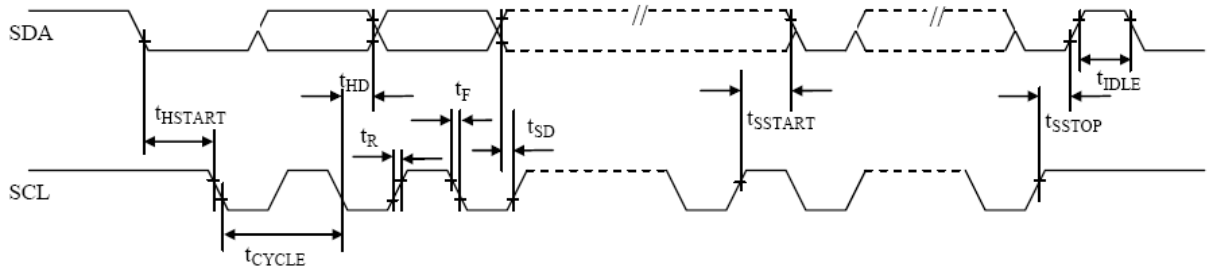


(4) I^2C interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I^2C interface Timing characteristics

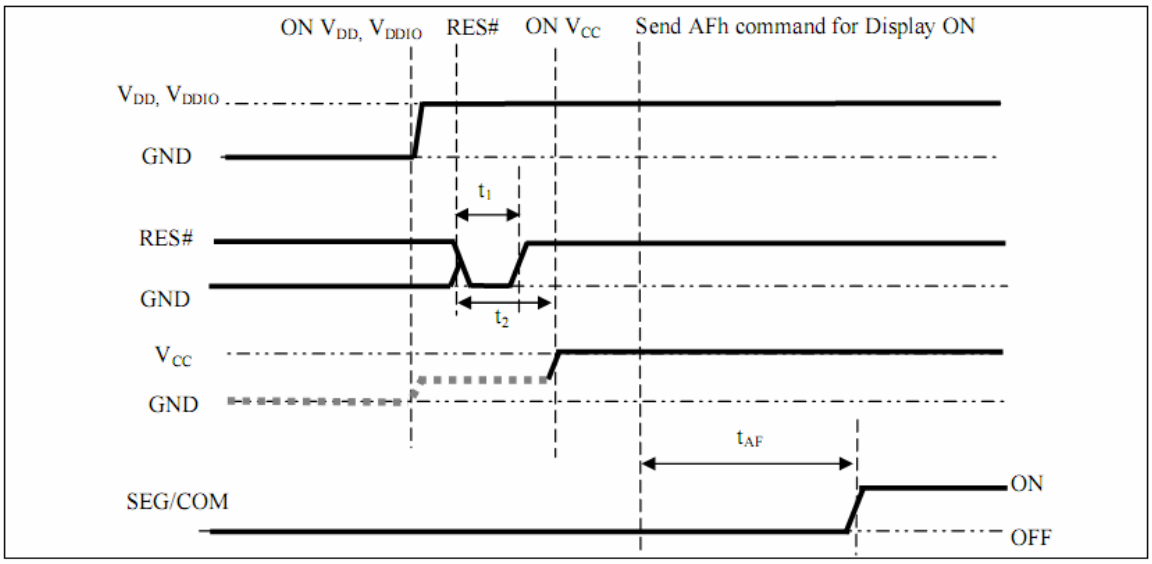


9 Functional Specification and Application Circuit

9.1 Power ON and Power OFF Sequence

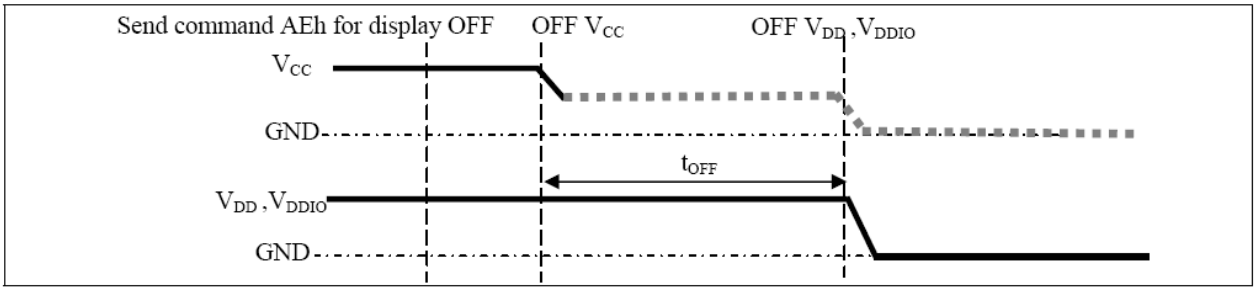
Power ON Sequence:

1. Power ON V_{DD},V_{DDIO}
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us (t_1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}[1].
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF Sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}[1],[2],[3].
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=0ms[5], Typical t_{OFF}=100ms)



Note:

(1)Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept float (disable) when it is OFF.

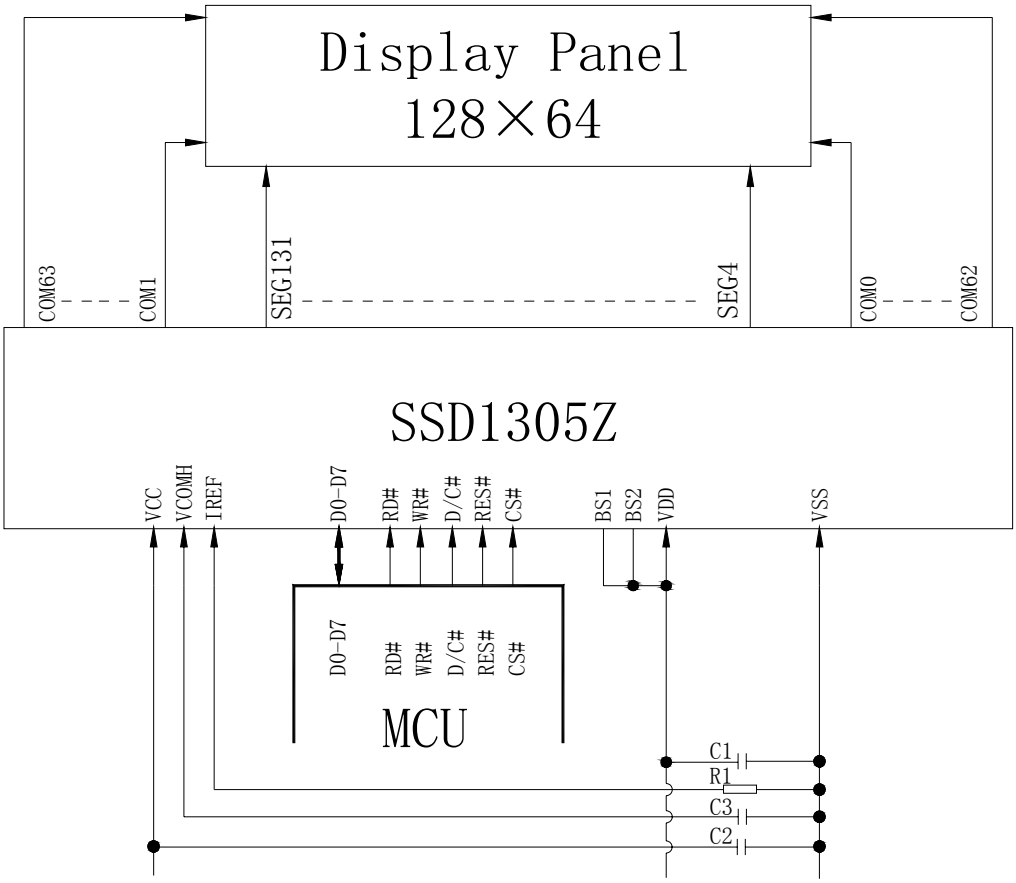
(3) Power Pins(V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{DD} should not be Power OFF before V_{CC} Power OFF

9.2 Application Circuit

The configuration for 8080-parallel interface mode, external VCC is shown in the following diagram:



Recommended components

C1~C3: 4.7μF

R1: 910kΩ, R1 = (Voltage at IREF - GND) / IREF

Voltage at IREF pin = VCC-3V

9.3 Display Control Instruction

Refer to SSD1305 IC Specification.

9.4 Recommended Software Initialization

TBD

10 Package Specification

Package order (1)~(9)

NOTE:Tape on the small carton & big carton

11 Reliability

11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	80℃,240hrs	4
2	Low Temperature (Non-operation)	-40℃,240hrs	4
3	High Temperature (Operation)	70℃,240hrs	4
4	Low Temperature (Operation)	-40℃,240hrs	4
5	High Temperature / High Humidity (Operation)	60℃,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40℃~80℃(-40℃/30min;transit/3min;80℃/30min;transit/3min) 1cycle: 66min,30cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
2. The degradation of polarizer is ignored for item 5.
3. The tolerance of temperature is ±3℃, and the tolerance of relative humidity is ±5%.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance:≥50% of initial value.
4. Current consumption: within ± 50% of initial value.

11.2 Lifetime

End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

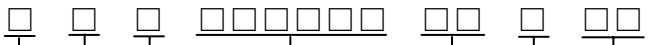
ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	TBD	-	hrs	100 cd/m^2,50% Checkerboard

An average operating lifetime of more than 10,000 hrs (checkerboard) at room temperature is approached by 240 hrs @ 80°C operating.

11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.

12 Illustration of OLED Product Name



Flow No. :

01~99

Display Color :

R—red

G—green

B—blue

Y—yellow

W—white

A—area color

F—full color

Panel Flow No. :

A0~A9, B0~B9…Z0~Z9

Display Format :

Graphic—columns and rows

Character—characters and line number

Segment—segment number

Icon—pixel number

Product Type :

P—panel

M—module

Display Type :

G—graphic

C—character

S—segment

I—Icon

M—mixed

Company :

V—Visionox

13 Outgoing Quality Control Specifications

13.1 Sampling Method

(1) GB/T 2828.1-2003/ISO2859-1：1999, inspection level Ⅱ, normal inspection, single sample inspection

(2) AQL: Major 0.65; Minor 1.0

13.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C

Humidity: 55±15%R.H

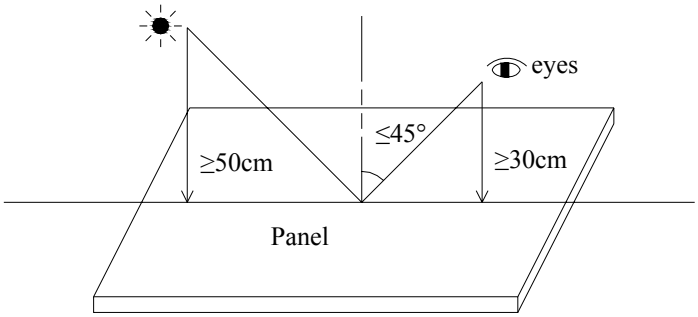
Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

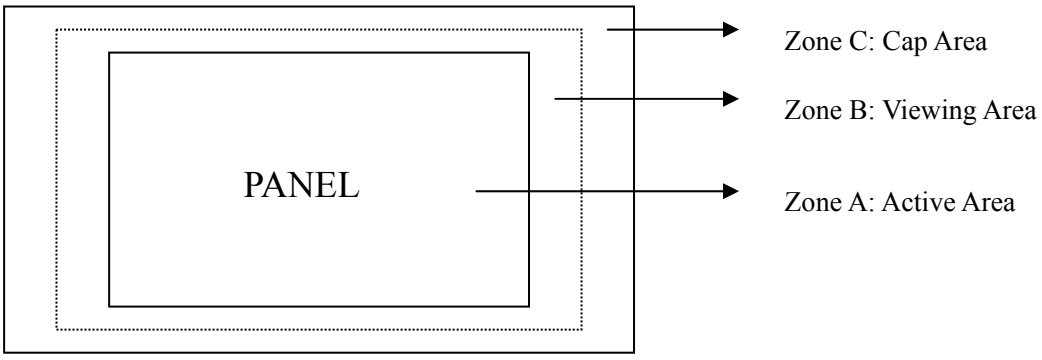
Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)

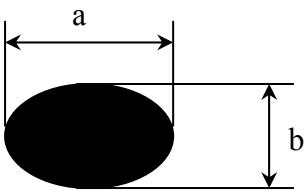


13.3 Quality Assurance Zones

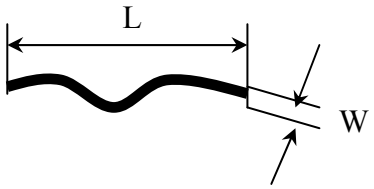


13.4 Inspection Standard

Definition of Φ&L&W (Unit: mm)

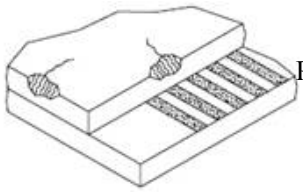
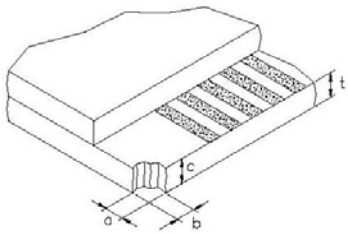
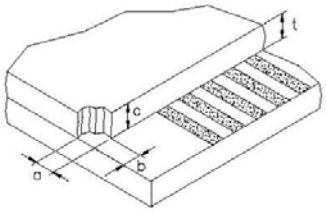
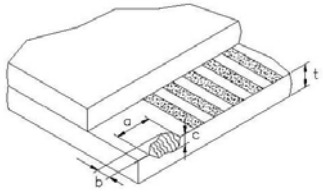
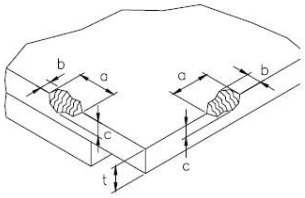
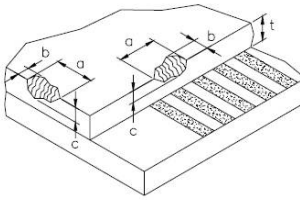


Φ=(a+b)/2



Ⅰ. Appearance Defects

NO.	ITEM	CRITERIA	CLASSIFICATION
1	Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer	<table><tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr><tr><td>Zone A,B</td><td>Zone C</td></tr><tr><td>Φ≤0.15</td><td>Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.15<Φ≤0.30</td><td>3</td></tr><tr><td>Φ>0.30</td><td>0</td></tr></table>	Minor
2	Scratch/line on the glass/Polarizer	<table><tr><td rowspan="2">Width (mm)</td><td rowspan="2">Length (mm)</td><td colspan="2">Acceptable Number</td></tr><tr><td>Zone A,B</td><td>Zone C</td></tr><tr><td>W≤0.03</td><td>---</td><td>Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.03<W≤0.08</td><td>L≤5.0</td><td>3</td></tr><tr><td>W>0.08</td><td>---</td><td>0</td></tr></table>	Minor
3	Polarizer Bubble	<table><tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr><tr><td>Zone A,B</td><td>Zone C</td></tr><tr><td>Φ>0.5</td><td>0</td><td rowspan="3">Ignore</td></tr><tr><td>0.2<Φ≤0.5</td><td>3</td></tr><tr><td>Φ≤0.2</td><td>Ignore</td></tr></table>	Minor
4	Any Dirt & Scratch on Polarizer's Protective Film	Ignore for not affect the polarizer.	Acceptable
5	Any Dirt on Cap Glass	<table><tr><td>Average Diameter (mm)</td><td>Acceptable Number</td></tr><tr><td>Φ≤0.5</td><td>Ignore</td></tr><tr><td>0.5<Φ≤1.0</td><td>3</td></tr><tr><td>Φ>1.0</td><td>0</td></tr></table>	Minor

5	Glass Crack	 Propagation crack is not acceptable.	Major
6	Corner Chip	 t= Glass thickness Accept a≤2.0mm or b≤2.0mm, c≤t	Minor
7	Corner Chip on Cap Glass	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
8	Chip on Contact Pad	 t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)	Minor
9	Chip on Face of Display	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
10	Chip on Cap Glass	 t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t	Minor
11	Stain on Surface	Stain removable by soft cloth or air blow is acceptable.	Minor
12	TCP/FPC Damage	(1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.	Minor
13	Dimension Unconformity	Checking by mechanical drawing.	Major

Ⅱ. Displaying Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Black/White spot
Dirty spot
Foreign matter</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Pieces Permitted</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.10</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td>3</td></tr>
<tr><td>Φ>0.20</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>No Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>3</td><td>Irregular Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>4</td><td>Missing Line
(row or column)</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>5</td><td>Short</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>6</td><td>Flicker</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>7</td><td>Abnormal Color</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>8</td><td>Luminance NG</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>9</td><td>Over Current</td><td>Refer to the SPEC.</td><td>Major</td></tr>
</table>

14 Precautions for operation and Storage

14.1 Precautions for Operation

(1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).

(2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.

(3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.

(4) Do not attempt to disassemble or process the OLED module.

(5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.

(6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

(7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.

(8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

14.2 Soldering

(1) Soldering should be performed only on the I/O terminals.
(2) Use soldering irons with proper grounding and no leakage.
(3) Iron: no higher than 300℃ and 3~4 sec during soldering.

14.3 Precautions for Storage

(1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
(2) Keep the environment temperature between 10℃ and 35℃ and the relative humidity less than 60%. Avoid high temperature and high humidity.
(3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.
(4) Do not leave any article on the OLED module surface for an extended period of time.

14.4 Warranty period

Visionox Display Co., Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition.